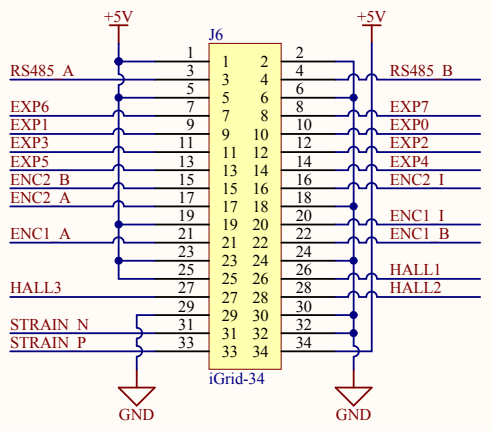
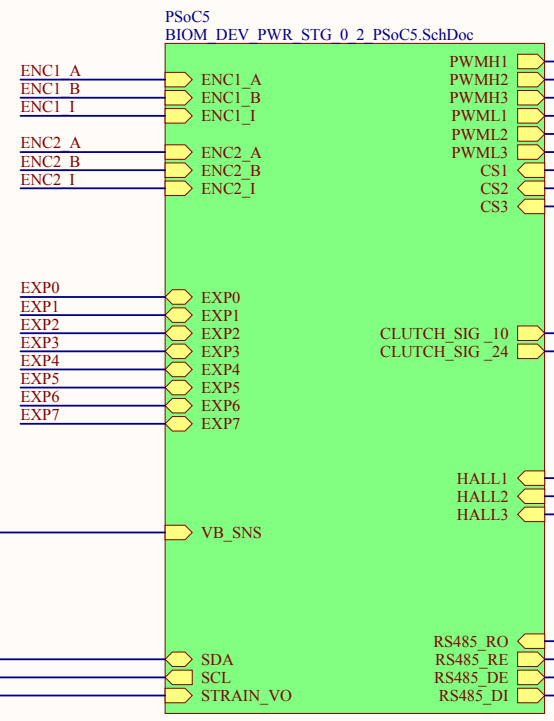


BIOM DEV PWR STG Motor Controller 24V 20A Max

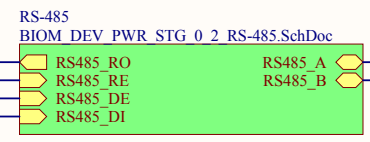
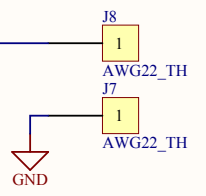
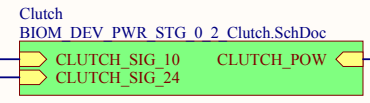
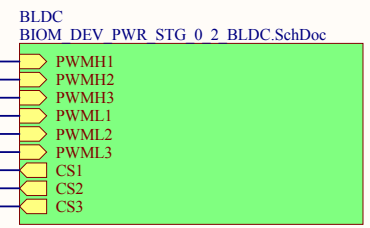
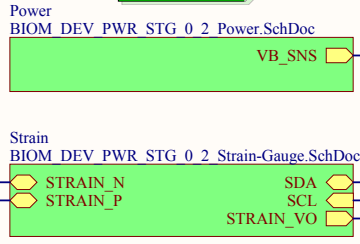
Logic Connector



PSoC 5LP



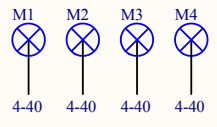
Regulators



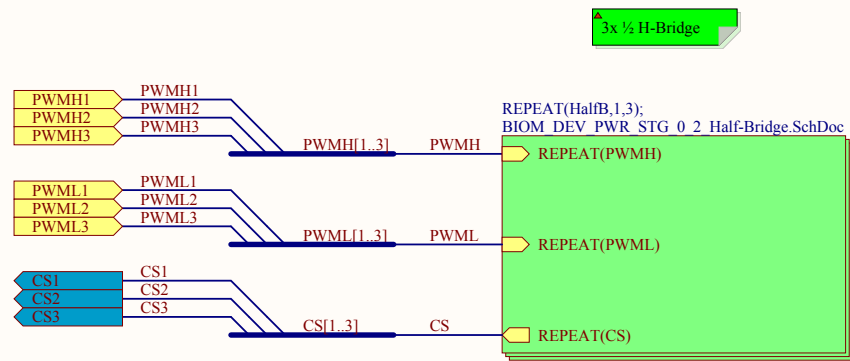
Future:


- ESD protections
- System safety

Can I use the PSoC to deal with the 2 SMPS? That could be interesting... One small LDO could be used for the boot. I could also synchronize the noise with the ADCs...

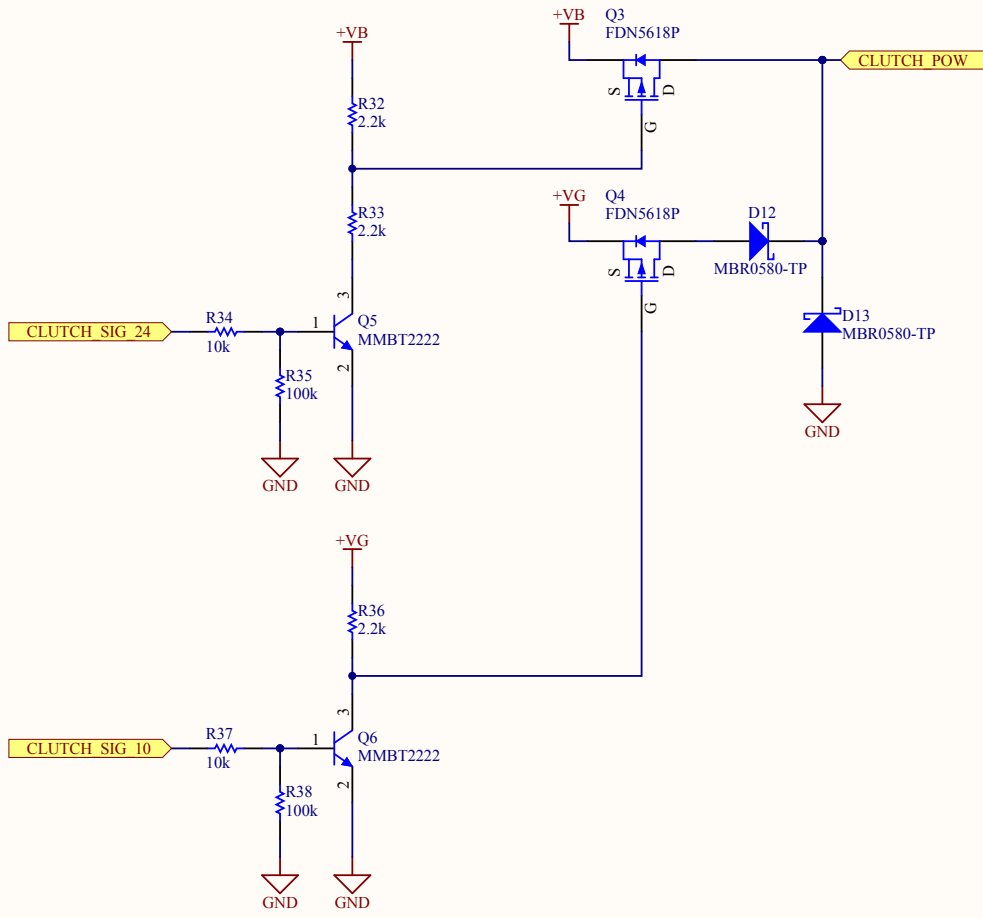



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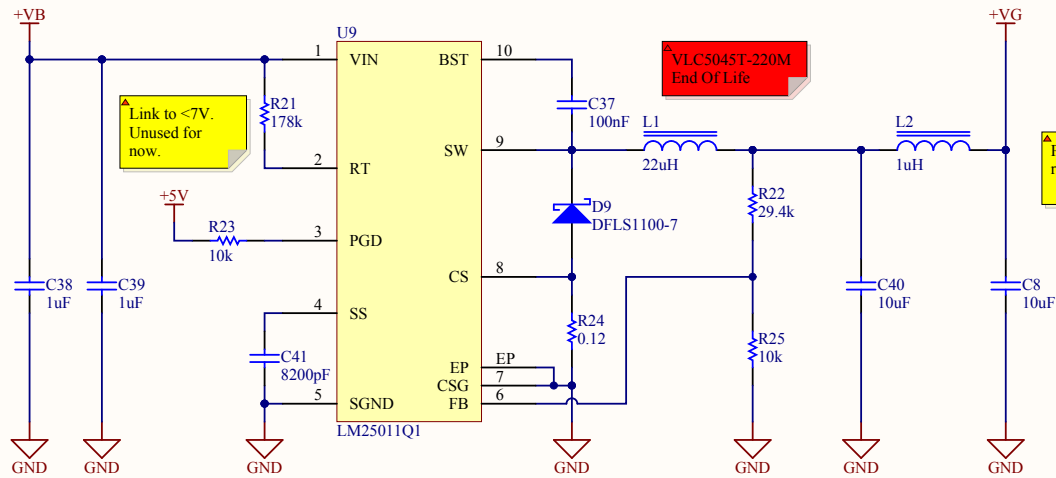
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10/24V Clutch



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10V 1A DC/DC




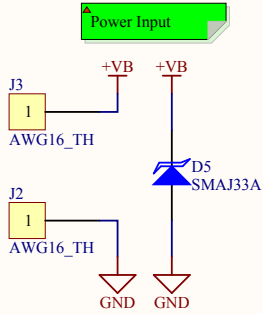
Link to <7V. Unused for now.

VLC5045T-220M End Of Life

Pi filter should reduce ripple by 10x

Max +VB: 42V

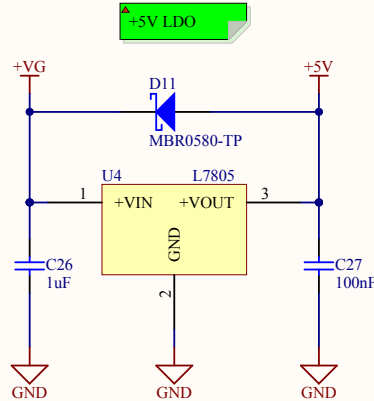
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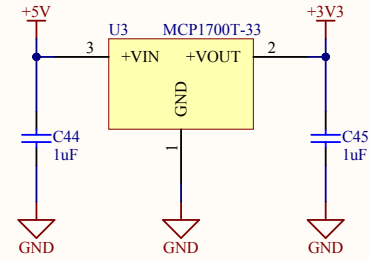
LM25011
BIOM_DEV_PWR_STG_0_2_LM25011_DCDC.SchDoc

TVS will clamp at min 36.7V and max 40.6V. The maximum tolerable voltage is determined by the LM25011 (42V)

+12V SMPS

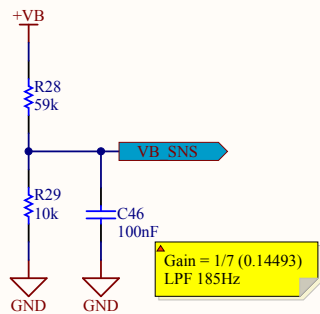


+3V3 LDO



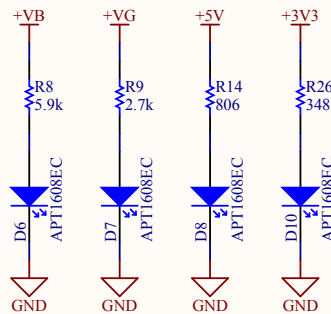
+3V3 only used for RS-485

Battery voltage

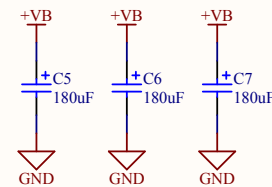


Gain = 1/7 (0.14493)
LPF 185Hz

Power LEDs

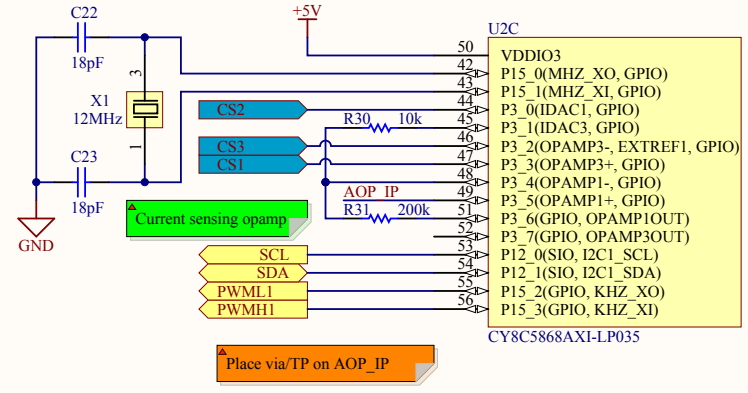
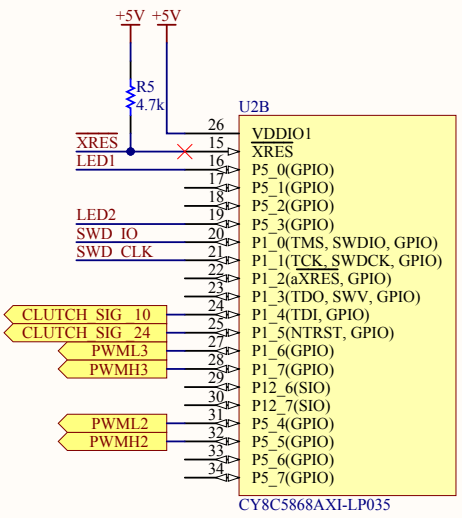
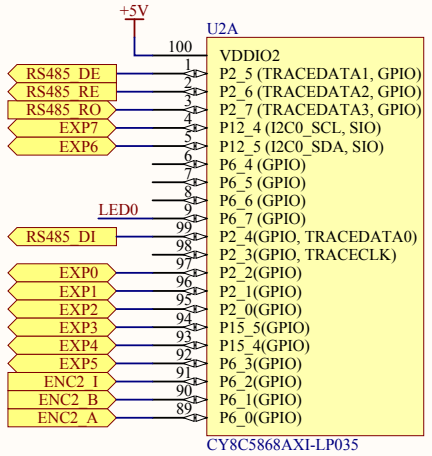
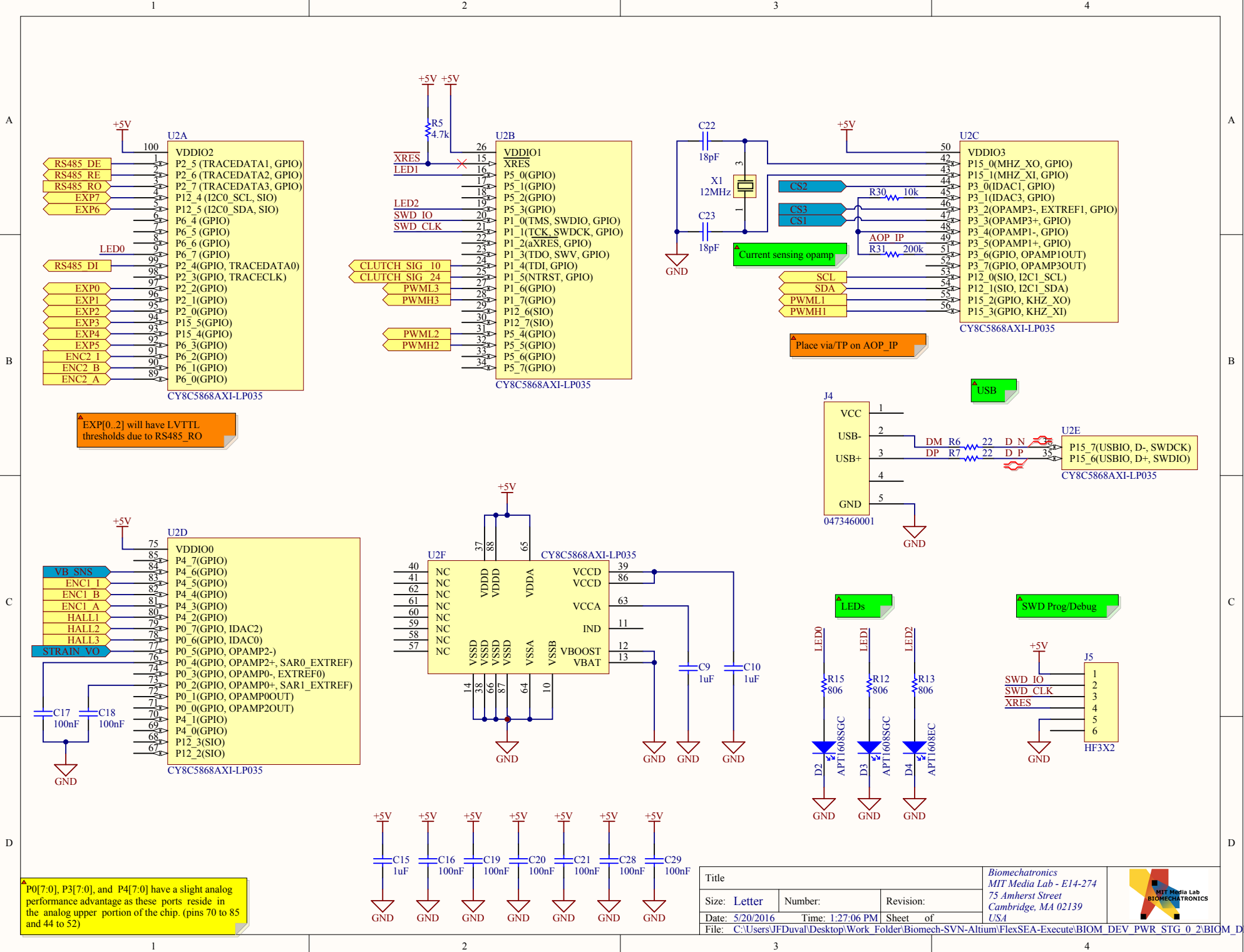


Power Decoupling

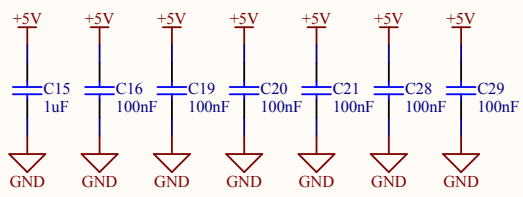
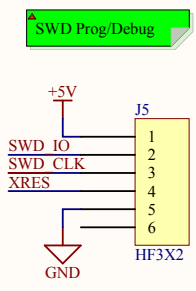
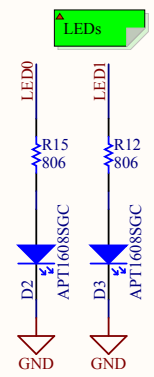
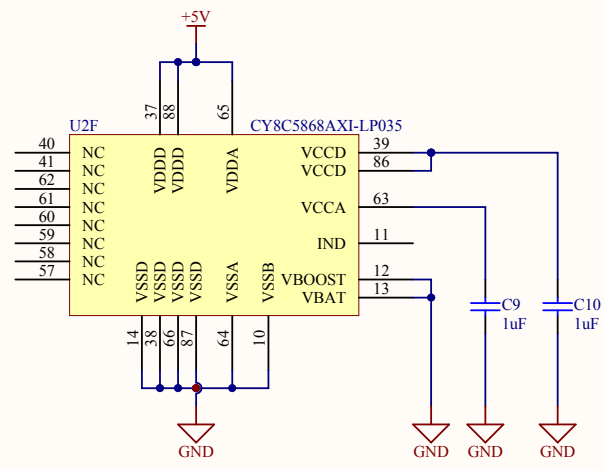
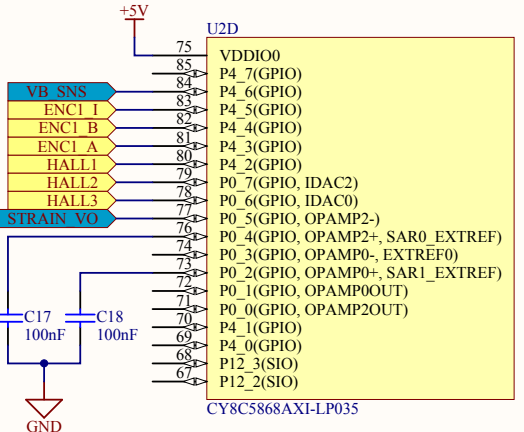
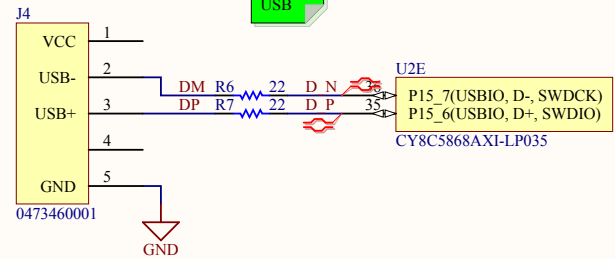


Naming convention:
 +VB x-xV (typ. 24V) Battery voltage
 +VG 10V Gate driver voltage, input for low voltage regulators
 +5V 5V Logic supply - almost everything
 +3V3 3.3V Logic supply - RS-485 transceiver

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▲ EXP[0..2] will have LVTTTL thresholds due to RS485_RO

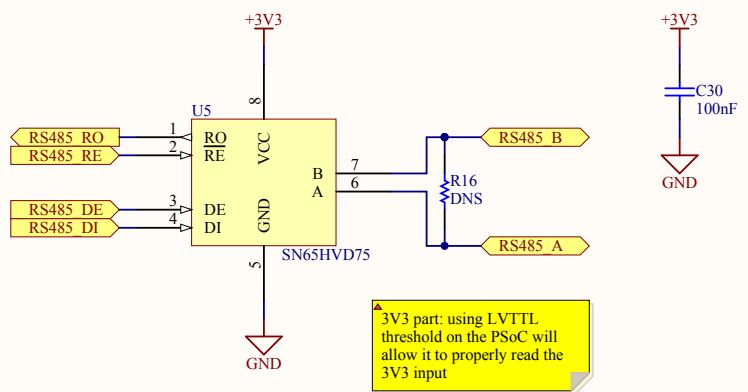


▲ P0[7:0], P3[7:0], and P4[7:0] have a slight analog performance advantage as these ports reside in the analog upper portion of the chip. (pins 70 to 85 and 44 to 52)

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RS-485 Transceiver



3V3 part: using LVTTTL threshold on the PSoC will allow it to properly read the 3V3 input

From datasheet:
 5V-Tolerant Logic Inputs Compatible With feature a wide common-mode voltage range making 3.3V or 5V Controllers
 *HVD75 is 20Mbps, *HVD72 for 250kbps
 Driver differential output voltage: min 1.5V, typ 2-2.5V

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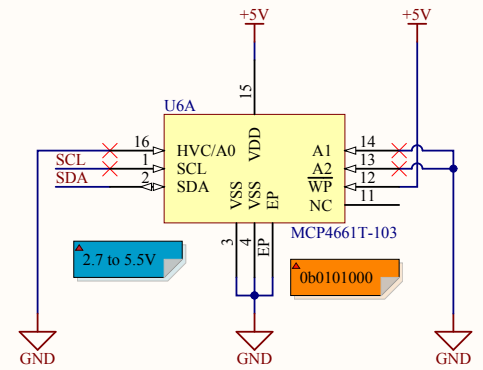
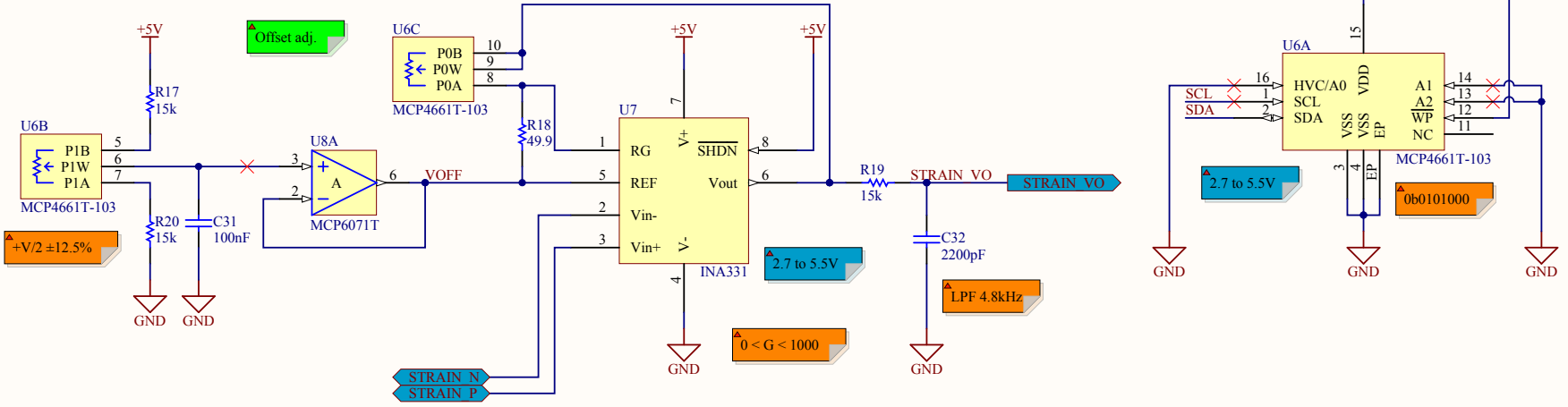


- FC programmable gain ($0 < G < 1000$) - 8 bits
 - FC programmable offset ($+V/2 \pm 12.5\%$) - 8 bits
 - Non-volatile settings
 - Unity gain for signals $0 < f < 1\text{kHz}$ ($f_c = 4.8\text{kHz}$)

Test!

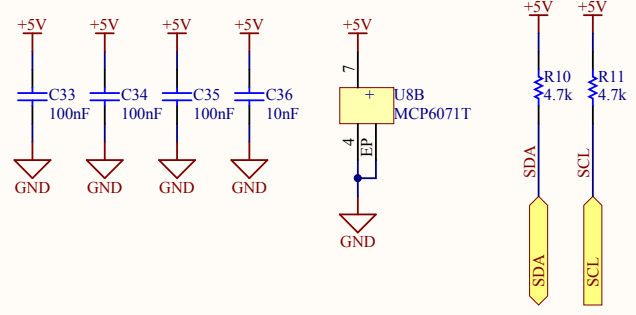
Variable Gain Instrumentation Amplifier

Digital pot.

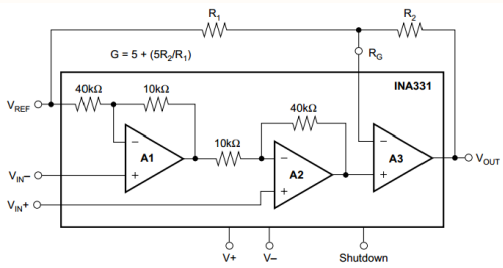


Decoupling

Decoupling



Low-noise wiring:
 - Add a shield to the cable. Link it to GND on the Strain Amp.
 - Make two twisted pair: excitation wires and signal wires
 For all the details please refer to
<http://www.vishaypg.com/docs/11051/tn501.pdf>



Title BIOM STRAIN AMP		Biomechatronics MIT Media Lab - E14-274 75 Amherst Street Cambridge, MA 02139 USA		
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